# LZ2324AK 1/3 type B/W CCD Area Sensor for CCIR

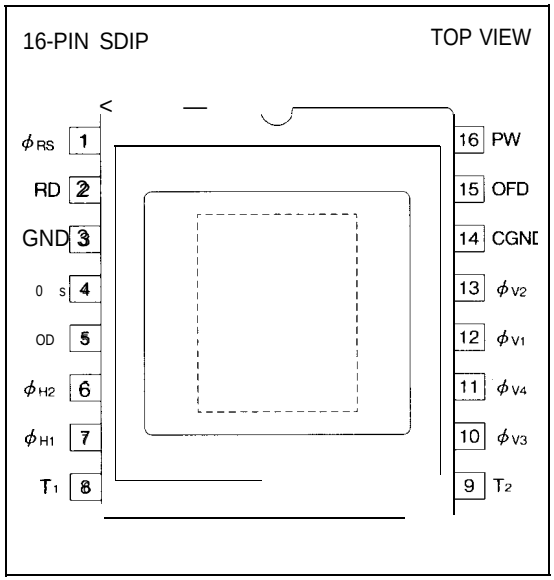
## DESCRIPTION

li!2324AK is a 1 /3-type (6.0 mm) solid-state image sensor that consists of PN phote-diodes and CCDS (charge-coupled devices). Having approxi-mately0000pixels (horizontal 542 Xvertical 582), the sensor provides a high resolution stable B/W image,

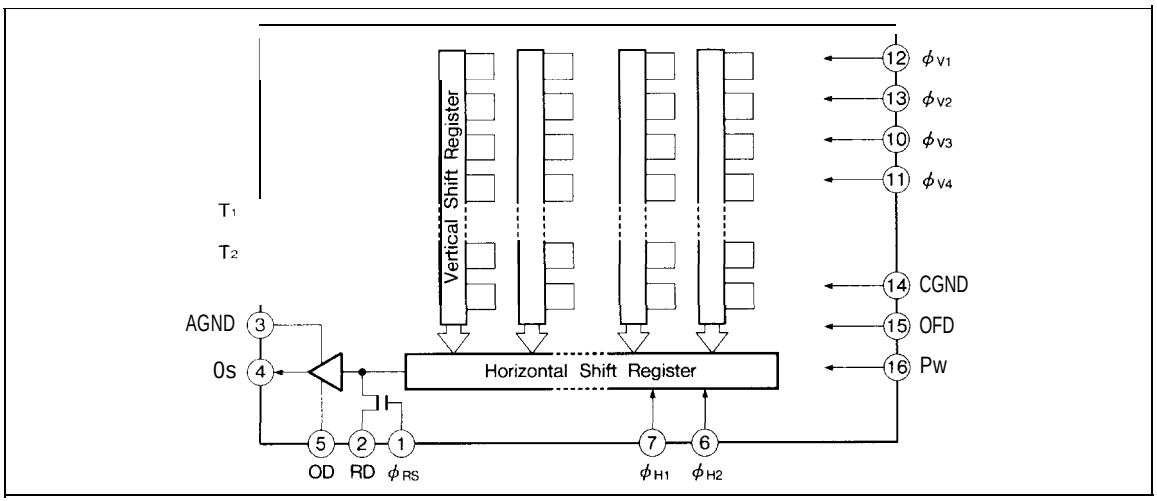
## FEATURES

- Number of pixels : 512 (H) X 582 (V)
  Pixel pitch : 9.6 $\mu$m (H) × 6.3 $\mu$m (V)
  Number of optical black pixels
  : Horizontal; front 2 and rear 28
- Low fixed pattern noise and lag
- No sticking and no image distortion
- Blooming suppression structure
- Built-in output amplifier
- Variable electronic shutter (1/50 to 1/1 O 000 s)
- Compatible with CCIR standard
- Package : 16-pin SDIP[CERDIP](WDIP016-N-0500C)

## PIN CONNECTIONS




## BLOCK DIAGRAM



## PIN DESCRIPTION

| SYMBOL | PIN NAME |
|---|---|
| RD | Reset transistor drain |
| OD | Output transistor drain |
| 0s | Video output |
| $\phi_{RS}$ | Reset transistor gate clock |
| $\phi_{V1}$, $\phi_{V2}$, $\phi_{V3}$, $\phi_{V4}$ | Vertical shift register gate clock |
| $\phi_{H1}$, $\phi_{H2}$ | Horizontal shift register gate clock |
| OFD | Overflow drain |
| Pw | P type well |
| AGND | Analog part ground |
| CGND | Clock part ground |
| $T_1$, $T_2$ | Test terminal |

## ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Output transistor drain voltage | $V_{OD}$ | Oto +18 | v |
| Reset transistor drain voltage | $V_{RD}$ | Oto +18 | v |
| Overflow drain voltage | $V_{OFD}$ | o to +55 | v |
| Test terminal. $T_1$ | $V_{T1}$ | Oto +18 | v |
| Test terminal, $T_2$ | $V_{T2}$ | –0.3 to +18 | v |
| Reset gate clock voltage | $V_{\phi RS}$ | –0.3 to +18 | v |
| Vertical shift register clock voltage | $V_{\phi V}$ | –9,0 to +18 | v |
| Horizontal shift resister clock voltage | $V_{\phi H}$ | –0.3 to +18 | v |
| Voltage difference between PW and vertical clock | $V_{PW}-V_{\phi V}$ | –27 to O | v |
| Storage temperature | Tstg | –20 to +80 | °C |
| Operating ambient temperature | Topr | –20 to +70 | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|
| Operating ambient temperature | | | Topr | | 25.0 | | °C | |
| Output transistor drain voltage | | | VOD | 14.5 | 15.0 | 16.0 | V | |
| Reset transistor drain voltage | | | VRD | | VOD | | V | |
| Overflow drain voltage | When DC is applied | | Vom | 5.0 | | 19.0 | V | 1 |
| | When pulse is applied p-p level | | Vφ OFD | 22.0 | | | V | 2 |
| Analog part ground | | | AGND | | 0,0 | | V | |
| Clock part ground | | | CGND | | 0.0 | | V | |
| P-well voltaae | | | VPW | – 9.0 | | Vφ VL | V | |
| Test terminal, T1 | | | VT1 | | VOD | | V | |
| Test terminal, T2 | | | VT2 | | 0.0 | | V | |
| Vertical shift register clock | | LOW level | Vφ V1L, Vφ V2L<br>Vφ V3L, Vφ V4L | – 8.5 | –8.0 | – 7.5 | V | |
| | | INTERMEDIATE level | Vφ V1I, Vφ V2I<br>Vφ V3I, Vφ V4I | | 0.0 | | V | |
| | | HIGH level | Vφ V1H, Vφ V3H | 16.0 | 16.5 | 17.0 | V | |
| Horizontal shift register clock | | LOW level | Vφ H1L, Vφ H2L | – 0.05 | 0.0 | 0.05 | V | |
| | | HIGH level | Vφ H1H, Vφ H2H | 4.7 | 5.0 | 6.0 | V | |
| Reset gate clock | | LOW level | Vφ RSL | 0.0 | | RD – 12.[ | V | |
| | | HIGH level | Vφ RSH | /RD – 7.5 | | 9,5 | V | |
| Vertical shift register clock frequency | | | fφ V1, fφ V2<br>fφ V3, fφ V4 | | 15,63 | | kHz | |
| Horizontal shift register clock frequency | | | fφ H1, fφ H2 | | 9.66 | | MHz | |
| Reset gate clock frequency | | | fφ RS | | 9.66 | | MHz | |

NOTES :

1. **When DC voltage is applied, shutter speed is 1 /50 seconds.**
2. **When pulse is applied, shutter speed is less than 1/50 seconds.**

## ELECTRICAL CHARACTERISTICS (Drive method : Field Accumulation)

**(T = 25°C, Operating conditions : typical values for the recommended operating conditions, Color temperature of light source : 3200 K / IR cut-off filter (CM-500, 1 mmt))**

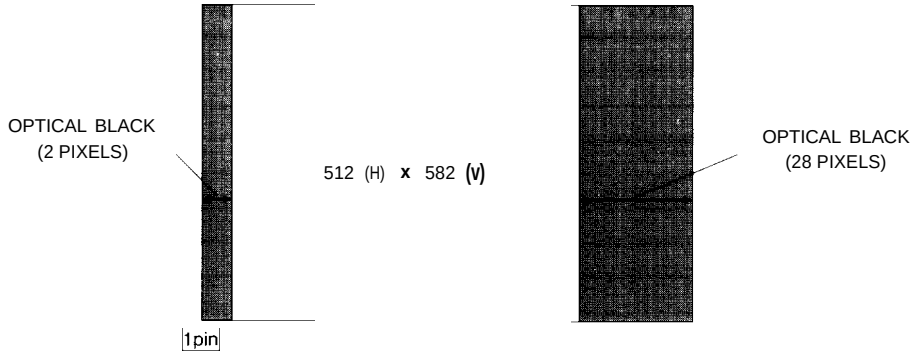
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|
| Photo response non-uniformity | PRNU | | | 10 | % | 2 |
| Saturation signal | Vsat | 550 | | | mV | 3 |
| Saturation non-uniformity | SSUN | | | 20 | % | 4 |
| Dark output voltage | Vdark | | 0,3 | 3.0 | mV | 1, 5 |
| Dark signal non-uniformity | DSNU | | 0.6 | 2,0 | mV | 1, 6 |
| Sensitivity | R | 360 | 500 | | mV | 7 |
| Gamma | Y | | 1 | | | |
| Smear ratio | SMR | | 0.009 | 0.016 | % | 8 |
| Image lag | AI | | | 1.0 | % | 9 |
| Blooming suppression ratio | ABL | 1000 | | | | 10 |
| Output transistor drain current | $I_{OD}$ | | 4.0 | 8.0 | mA | |
| Output impedance | Ro | | 300 | | Ω | |
| Dark noise | Vnoise | | 0.2 | 0,4 | mV | 11 |
| OB difference in level | | | | 1,0 | mV | 12 |

- The standard output voltage is defined as 150 mV by the average output voltage under uniform illumination.
- The standard exposure level is defined when the average output voltage is 150 mV under uniform illumination.

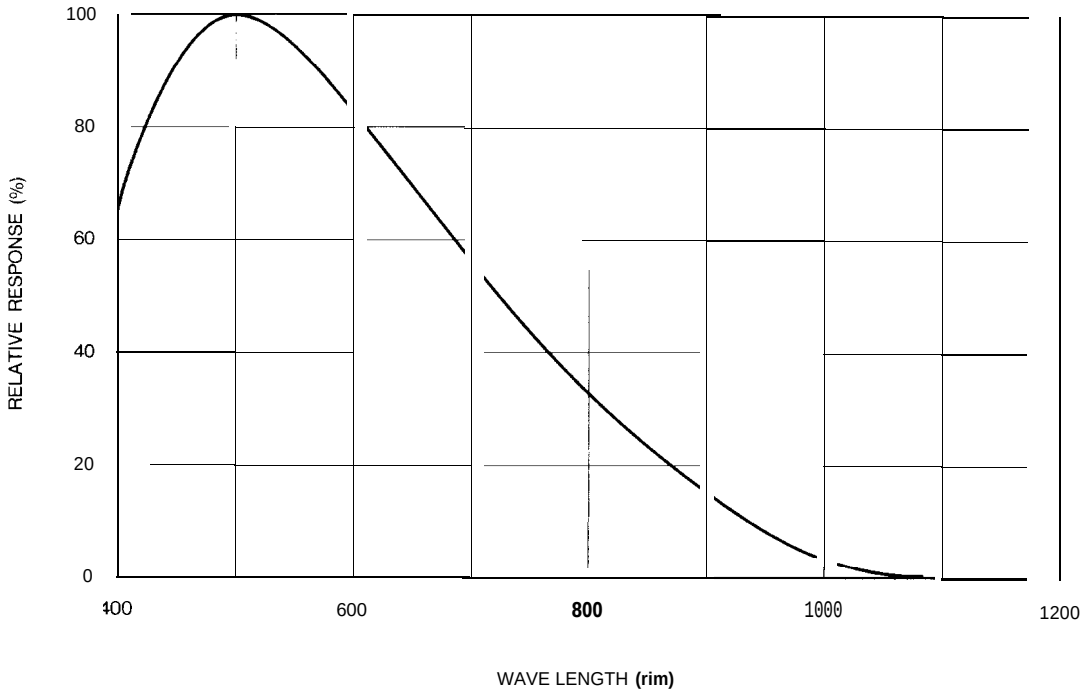
**NOTES :**

1. Ta : +60°C
2. The image area is divided into 10X 10 segments. The segment's voltage is the average output voltage of all the pixels within the segment. PRNU is defined by (Vmax – Vmin)/Vo, where Vmax and Vmin are the maximum and the minimum values of each segment's voltage respectively, when the average output voltage Vo is 150 mV.
3. The image area is divided into 10x 10 segments. The saturation signal is defined as the minimum of each segment's voltage which is the average output voltage of all the pixels within the segment, when the exposure level is set as 10 times, compared to standard level.
4. The image area is divided into 10X 10 segments. The voltage of a segment is the saturation signal (Vs), when the exposure level is set as 10 times, compared to standard level. SSUN is defined by (Vmax– Vmin)/Vs, when Vmax and Vmin are the maximum and minimum values of each segment's voltage respectively.
5. The average output voltage under a non-exposure condition.
6. The image area is divided into 10X 10 segments. DSNU is defined by (Vdmax – Vdmin) under the non-exposure condition where Vdmax and Vdmin are the maximum and the minimum values of each segment's voltage, respective y, that is the average output voltage over all pixels in the segment.
7. The average output voltage when a 1 COO luxl ight source attached with a 90% reflector is imaged by a lens of F4, f50 mm.
8. The sensor is adjusted to position a V/l O square at the center of image area where V is the vertical length of the image area. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the pixel voltage in the V/l O square.
9. The sensor is exposed at the exposure level corresponding to the standard condition preceding non-exposure condition. AI is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.
10. The sensor is adjusted to position a V/l O square at the center of image area. ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.
11. The RMS value of the dark noise (after CDS). The bandwidth range is from 100 kHz to 5.0 MHz
12. The difference between the average output voltage of the effective area and the OB part under the non-exposure condition.

## PIXEL STRUCTURE




## SPECTRAL RESPONSE EXAMPLE

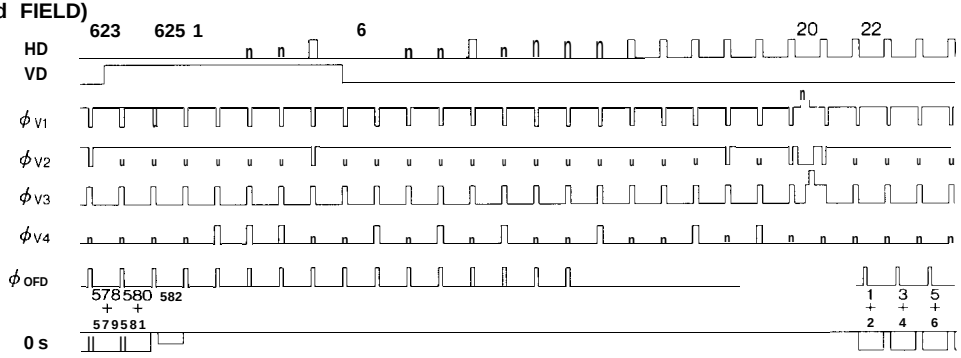


## TIMING DIAGRAM EXAMPLE

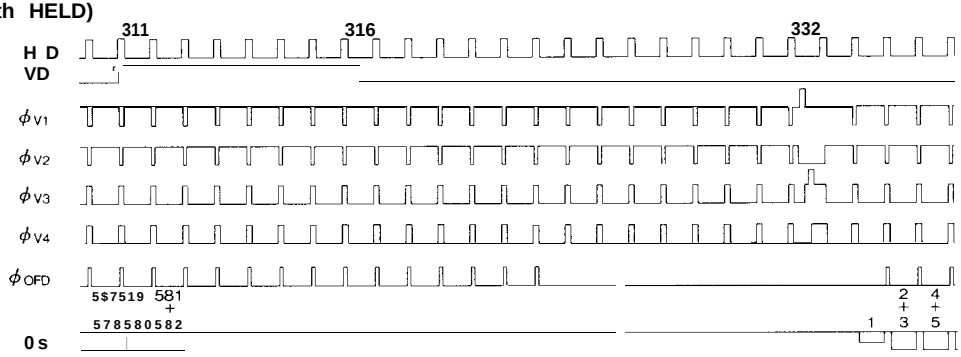
VERTICAL TRANSFER TIMING

Shutter speed 1/2000 s

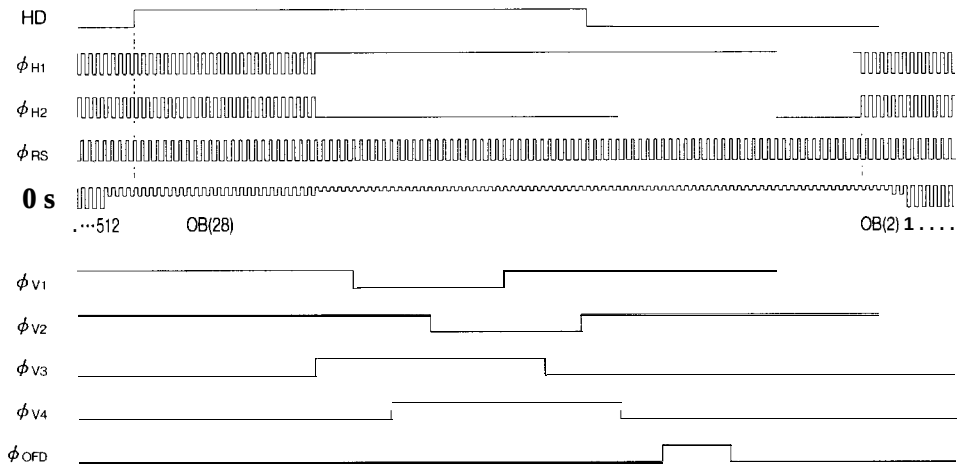
(1st, 3rd FIELD)




(2nd, 4th HELD)



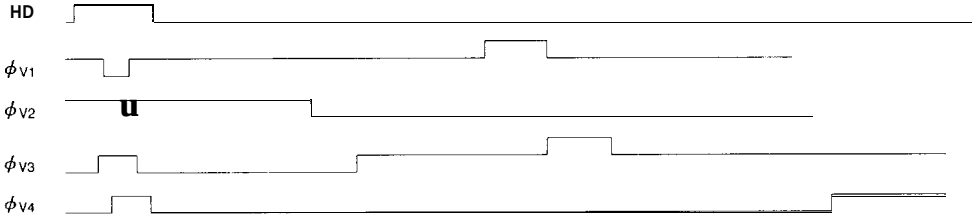

HORIZONTAL TRANSFER TIMING



## READOUT TIMING

**(Ist, 3rd FIELD)**


**(2nd, 4th FIELD)**



## SYSTEM CONFIGURATION EXAMPLE